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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/400,508	09/20/99	ALLEE	D 2000.000900

EXAMINER	
CHO, T	
ART UNIT	**PAPER NUMBER**
2819	

MMC2/0308

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DATE MAILED: 03/08/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/400,508	Allee
Examiner	**Group Art Unit**
James H. Cho	2819

☒ Responsive to communication(s) filed on *Jan 26, 2001*

☒ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *1-16* is/are pending in the applicat

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-16* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

1. Receipt is acknowledged of the Amendment filed January 26, 2001.

Claim Objections

2. Claims 2-10 and 12-16 are objected to because of minor informalities:

The wording, "A logic", on line 1 of claims 2-10 and 12-16 appears to be --The logic-- respectively.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Lee (US PAT. 6,078,194). Lee shows and teaches all the elements and means of the claimed invention of the claim 1:

Lee teaches a logic gate (see Fig. 4(a) and 4(b)), comprising: a low noise current source (see 32) coupled between a first terminal of a voltage supply (see Vcc) and an output terminal (see OUT in Fig. 1), the low noise current source being capable of delivering a preselected voltage signal to the output terminal having a magnitude responsive to a first control signal (see

PEN) relatively independent of the magnitude of the voltage on the first terminal of the voltage supply, and at least one switching element (see 36 and 38) coupled between the output terminal and a second terminal (see VTT) of the voltage supply, the switching element being capable of coupling the output terminal to the second terminal of the voltage supply in response to receiving a control signal (see A or B).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (US PAT. 6,078,194).

Lee discloses the logic gate as set forth in claim 1 where the low noise current source includes a transistor (see 32) and a second transistor (see 34) whose gate is connected to the source serially coupled between the first terminal of the voltage supply and the output terminal, the transistor having a gate capable of receiving the first control signal, but does not discloses the second transistor being a resistor.

However, it is well known in the art that the second transistor is configured as a diode and the diode configured transistor is recognized as equivalent to a resistor in this environment.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have replace the second transistor of Lee with a resistor for the purpose of reducing through current.

7. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over modified Lee (US PAT. 6,078,194).

Regarding claim 16, the modified apparatus of Lee as applied to claim 2 discloses the logic gate as discussed above and an n-type transistor but does not disclose the transistor is a p-type transistor.

However, an n-type transistor is logically equivalent to a p-type transistor with its gate coupled to an inverter for the switching function. A substitution of such an equivalence is generally recognized as being within the level of ordinary skill in the art.

Therefore, it would have been an obvious engineering choice to replace an n-type transistor with a p-type transistor with its gate coupled to an inverter. As a matter of engineering choice, a p-type transistor has a lower transconductance than an n-type transistor so that the p-type transistor provides higher driving current.

8. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (US PAT. 6,078,194) in view of Chang et al. (US PAT. 5,955,893).

Lee discloses the logic gate, as set forth in claim 1 but does not disclose the transistor is an intrinsic transistor.

However, Chang et al. discloses an intrinsic transistor (see 508 in Fig. 6) for the purpose of providing a transistor having a lower magnitude of threshold voltage.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to combine the transistor of Lee with the intrinsic transistor of Chang et al. because it would provide full voltage at the output terminal since the threshold voltage of the intrinsic transistor is lower than non-intrinsic transistor.

9. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (US PAT. 6,078,194) in view of Thompson et al. (US PAT. 3,651,334).

Lee discloses the logic gate, as set forth in claim 1 but does not disclose a capacitor coupled between the output terminal and the second terminal of the voltage supply.

However, Thompson et al. discloses a capacitor (see 28 in Fig. 1) coupled between the output terminal and the ground for the purpose of providing charging the output node.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to combine the logic gate of Lee with the capacitor of Thompson because it would provide a precharged voltage.

10. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (US PAT. 6,078,194) in view of Sundstrom (US PAT. 5,602,494).

Lee discloses the logic gate, as set forth in claim 1 but does not disclose at least one clamping diode coupled between the output terminal and the second terminal of the voltage supply.

However, Sundstrom discloses a clamping diode (see 142 in Fig. 2) coupled between the output terminal and a second terminal for the purpose of providing input protection.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to combine the logic gate of Lee with the clamping diode of Sundstrom because it would provide input protection from an external terminal.

11. Apparatus claims 6-15 are essentially the same in scope as rejected apparatus claims 1-5 and 16 and are rejected similarly.

Response to Amendment

12. Applicant's arguments filed January 26, 2001 have been fully considered but they are not deemed to be persuasive regarding claims 1-9 and newly added claims 10-16.

On page 4 of the amendment, applicant argues that "Lee does not show or suggest a low noise current source that ... a preselected voltage signal to its output terminal that has a magnitude responsive to a first control signal relatively independent ..." and "the transistor (32) of Lee is an n-type transistor ...". However, the examiner notes that there is no specific recitation in the rejected claims 1-9 that the transistor is a p-type transistor. For newly added claims 10-16 the equivalence of a p-type transistor to an n-type transistor with its gate coupled to an inverter is

well known in the art as discussed above and does not change the logic function of the circuit. Furthermore, the examiner notes that the n-type transistor of Lee provides a relatively low current source and relatively independent of the magnitude of the voltage on the voltage supply by the control signal, PEN compared to other noisy current sources.

Additional Remark

13. It is noted from applicant's remark on page 3, line 10+ that applicant stated the terms "the and "said" are interchangeably used to refer back to an earlier introduced noun and objections were withdrawn.

14. The Office action in the paper number 2 has a minor typographical error on page 3, line 7; the wording "102(b)" should be "102(e)" as stated on the page 3, lines 2-5.

Conclusion

15. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kumar (US PAT. 5,426,383) discloses a high performance logic circuit, NCMOS.

Honma (US PAT. 4,697,109) discloses a level converter circuit.

Contact Information

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ***James H. Cho*** whose telephone number is (703)306-5442. The examiner can normally be reached between the hours of 5:30 AM to 2:30 PM Monday thru Friday.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

James H. Cho
Patent Examiner, Art Unit 2819
March 1, 2001

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